



JAMES COOK UNIVERSITY

Faculty of Science Engineering and IT

School of Engineering

SUBJECT OUTLINE

EE4306 Electronics 3

(Semester 2, 2004)

Campus: **Townsville** Mode of Offering: **Internal**

HANDBOOK DESCRIPTION:

Electronics 3, Townsville, HECS Band 2

39 hours lectures, 39 hours tutorials, demonstrations and practicals, site visits and seminars. Semester 2.

Asynchronous sequential logic design. VHDL programming language, applications and design. Isolating amplifiers, DC-DC converters, noise in amplifiers. RF transformers, transformer and stripline combiners and couplers. Mixers. Local oscillators for LF to SHF. Impedance matching and power amplifiers. RF component computer simulation and design optimisation. PCB technology, design tools, cost factors and limitations. Thick film and thin film techniques.

LEARNING OBJECTIVES AND OUTCOMES:

demonstrate an understanding of the use and design of asynchronous sequential logic circuits;

demonstrate an understanding of and a capability for the design of RF electronic circuits;

demonstrate an ability in using VHDL and CPLD and FPGA design tools to program and design CPLD and FPGA circuits;

demonstrate a knowledge of PCB design tools and materials for both RF and conventional boards;

present, explain and justify the components and techniques used in an RF design.

Assessment by examination (50%-70%); on-course assessment (30%-50%).

STAFF:

Lecturer	Room #	Consultations	Email contact	Telephone
A/Prof. Keith Kikkert	EL110	Open door policy	Keith.kikkert@jcu.edu.au	4781 4259

CLASS TIMES:

Lectures and Tutorials

Tuesday	11 am	Lecture	EL006
Tuesday	1 pm	Tutorial	EL201/EL209
Wednesday	1 pm	Tutorial	EL006/EL209
Friday	9 am	Lecture	EL006
Friday	10 am	Lecture	EL006
Friday	11 am	Tutorial	EL006

Note: one of the tutorial slots will not be used after consultation with the class to minimise clashes.

Practicals

Thursday 9 am - 12 noon

2 September	E4301 VHDL Introduction	EL209
9 September	E4302 Asynchronous Logic with VHDL	EL209
7 October	E4303 RF Simulation	EL209
14 October	E4304 RF Transformers and Mixers	EL007

ATTENDANCE REQUIREMENTS:

Attendance at all assigned class times is expected. You are responsible for all information (both technical and administrative) presented during class times. You should establish informal study groups and one function of these is to give you access to information, if for any reason, you miss a class session.

There is a very high correlation between attendance at lectures, tutorials and practicals with pass-rate.

TEXT BOOK/S:

None

REFERENCE TEXTS AND JOURNAL ARTICLES:

J. Basker *VHDL Primer (3rd Ed)*, Prentice Hall, 1999
D. Pozar *Microwave Engineering*, 3rd Ed Wiley, 2005

You are strongly encouraged to purchase Basker as a reference VHDL book. Much reference material in the form of manufacturers data and application notes is available on the subject web site.

TEACHING SUPPORT MATERIALS:

This subject will use **LearnJCU** which is available through **StudentsONLINE** on the JCU web site via Current Students and the subject web pages at: <http://eng.jcu.edu.au/subjects/ee4306/>

ESTIMATE OF TIME REQUIRED FOR THIS SUBJECT

The number of class hours in any one week will vary depending on the scheduling of practicals. There will be 3 hours of lecture and an average of one and a half hours of tutorial each week and the four practicals will require typically three hours preparation each. Self study outside of class periods will vary from student to student, but you should expect to spend *at least* 6 hours of study in addition to class time each week.

ASSESSMENT:

For information on the award of grades, policy on supplementary and deferred examinations see the School of Engineering web page <http://www.eng.jcu.edu.au/resources/studentinfo/>.

Exam (50%). One, 2-hour exam will cover all aspects of the subject. The primary emphasis will be to test if the student has an understanding of the material outlined in this course, is able to articulate this understanding and is able to apply this knowledge to solve engineering problems.

Assignments (30%). There will be two assignments, one for VHDL worth 10% of the total subject mark and one an RF design worth 20% of the total subject mark.

Assignment Due dates:

VHDL	10am Monday 13 September	worth 10% of total mark
RF design	10am Monday 18 October	worth 20% of total mark

Practicals (15%). There are four practical sessions for this subject. The practicals require **preparation, participation and individual reporting**. Three practicals will be marked in class and one will be required to be written up as a full report. The guidelines for format for lab conduct and the lab preparation and reports is available on the JCU web at: <http://eng.jcu.edu.au/subjects/ece4labs/PracProcedures.PDF>. The practical

session that is written up is worth 6% of the total course marks and the others are worth 3% each. Late submissions will receive a penalty as outlined up to a 100% penalty.

Safety is a very important consideration during practicals. Please see *Safety Requirements for Engineering Buildings* on the School of Engineering web pages at <http://www.eng.jcu.edu.au/resources/studentinfo/>.

Tutorial Participation (5%). Some tutorial problems should be done by the student outside the tutorial periods, and the tutorial sessions are used to go through the solution of that problem. For some of these (selected at random) a mark will be given for the attempt done by the student.

ASSESSMENT CRITERIA:

The criteria for assessment of the assignment will be included as part of the assignment document. The criteria for assessment of the practical sessions are available on the laboratory web site. <http://eng.jcu.edu.au/subjects/ece4labs/PracProcedures.PDF>

SUBMISSION OF ASSIGNMENTS:

The practical report must be submitted directly to the lecturer. Any assignment required to be submitted in hard copy are to be submitted directly to the lecturer, any assignment required to be submitted electronically is to be submitted through the dropbox in **LearnJCU** on or before the due date. Late submissions are penalised by 15% per week or part thereof. The marks awarded will be placed on the JCU web site.

PLAGIARISM:

Plagiarism is the act of using another's words, works or ideas from any source as one's own. Plagiarism has no place in a University. Student work containing plagiarised material will be subject to disciplinary action and may result in exclusion from the University. The University Policy on Plagiarism may be found in the JCU Student Handbook 2004, or web pages: <http://www.jcu.edu.au/courses/handbooks/2004/exam.html> Students should also be aware of the JCU policies relating to Student Academic Misconduct (cheating) found at the same web address.

For help in avoiding plagiarism see: <http://www.jcu.edu.au/studying/services/studyskills/reference/>

FINAL GRADE:

The raw marks that you receive from each piece of assessable material will be combined into a total mark for the subject. These raw marks may undergo a scaling process to ensure meeting School and University policies on the distribution of grades. Please see *Assessment Policy* on the School of Engineering web pages at <http://www.eng.jcu.edu.au/resources/studentinfo/>.

DEFERRED EXAM:

The award of a deferred examination is *not* automatic even if a valid medical excuse is presented. A request for a deferred examination may be refused if the student has a poor record of participation (e.g. failure to attend mandatory sessions, or failure to submit *all* assessable material). Please see *Deferred Assessment Policy* on the School of Engineering web pages at <http://www.eng.jcu.edu.au/resources/studentinfo/>.

WORKPLACE HEALTH AND SAFETY:

The University staff, management and students have mutual obligations in relation to maintaining a safe workplace and learning environment. Students are required to follow directions specific to sites and safety procedures as directed by staff. Failure to follow safety instructions may result in that person being denied access to the facilities. Please see School policy at:

http://www.eng.jcu.edu.au/resources/studentinfo/safety_requirements.html

STUDENT SUPPORT:

Some students will have problems that can span a wide range of family, relationship, health, emotional, financial and educational issues. Both the School and University have support systems. We can help, but if problems occur you must seek help promptly. See your lecturer, Professor Tom Hardy, Associate Dean (Engineering), or contact Student Services via the web page <http://www.jcu.edu.au/studying/services/>

STUDENTS WITH DISABILITIES:

Students with a disability who require special arrangements or consideration should contact Professor Tom Hardy, Associate Dean (Engineering) and the Disability Resource Officer in the Equal Opportunity Unit (Ph: 4781 5152).

Course Outline

Digital Electronics

VHDL programming language	
Language structure, Examples and hardware realisation	4 Lectures
Compilers and software	1 Lecture
Hardware Realisation, pin allocation	1 Lecture
Examples	2 Lectures
Asynchronous sequential logic design:	
Problem Formulation, Logic Signal Flow Graph	2 Lectures
Examples	1 Lecture
Realisation Procedure using VHDL	1 Lecture
Phase Locked Loop Techniques	
Phase Detectors using synchronous and asynchronous logic	1 Lecture

RF Electronics

Introduction	
RF Computer Simulation and design optimisation	2 Lectures
RF Transformers and hybrids	2 Lectures
Transmission line impedance matching	1 Lecture
Stripline combiners and couplers: Wilkinson, Ratrace, Branchline, Backward wave, Lange	2 Lectures
Mixers, Single diode, Balanced, Double balanced, IQ and active	3 Lectures
Local Oscillators LF to SHF RC, LC, Cavity Oscillators, Crystal Oscillators	3 Lectures
Low Power Amplifiers: IF amplifiers, low noise amplifiers, noise and stability circles	2 Lectures
RF Power Amplifiers, input and output impedance, configurations	1 Lectures
LC and Stripline Matching	2 Lectures
RF amplifier design example	1 Lecture
RF Filters	3 Lectures
High speed operational amplifiers and Noise in op amps	2 Lectures
Design and production trends in RF instrumentation	2 Lectures